

## CLAIMS

### WHAT IS CLAIMED:

1. A built-in self-test controller, comprising:  
a built-in self-test engine capable of executing a built-in self-test and generating an indication of whether the executed built-in self-test is completed; and  
a built-in self-test signature including the indication.

2. The built-in self-test controller of claim 1, wherein the built-in self-test engine is a logic built-in self-test engine and the built-in self-test signature is a logic built-in self-test signature.

3. The built-in self-test controller of claim 2, wherein the logic built-in self-test engine comprises:  
a logic built-in self-test state machine; and  
a pattern generator.

4. The built-in self-test controller of claim 3, wherein the logic built-in self-test state machine further comprises:  
a reset state entered upon receipt of an external reset signal;  
an initiate state entered from the reset state upon receipt of a logic built-in self-test run signal;  
a scan state entered from the initiate state upon the initialization of components and signals in the logic built-in self-test domain in the initiate state;  
a step state entered into from the scan state and from which the scan state is entered unless the content of the pattern generator equals a predetermined vector count; and  
a done state entered into when the content of the pattern generator equals the predetermined vector count.

5. The built-in self-test controller of claim 1, wherein the logic built-in self-test signature comprises the content of a multiple input signature register.

1           6.       The built-in self-test controller of claim 1, wherein the built-in self-test engine  
2 is a memory built-in self-test engine and the built-in self-test signature is a memory built-in  
3 self-test signature.

1           7.       The built-in self-test controller of claim 6, wherein the memory built-in self-  
2 test signature includes the results of at least one paranoid check.

1           8.       The built-in self-test controller of claim 6, wherein the memory built-in self-  
2 test signature includes a bit indicating whether a memory built-in self-test is done.

1           9.       The built-in self-test controller of claim 6, wherein the memory built-in self-  
2 test engine comprises:

3           a memory built-in self-test state machine; and  
4           a nested memory built-in self-test engine operating the memory built-in self-test state  
5           machine.

1           10.      The built-in self-test controller of claim 9, wherein the memory built-in self-  
2 test state machine comprises:

3           a reset state entered upon receipt of an external reset signal;  
4           an initiate state entered from the reset state upon receipt of at least one of a memory  
5           built-in self-test run signal and a memory built-in self-test select signal;  
6           a flush state entered from the initiate state upon the initialization of components and  
7           signals in the memory built-in self-test domain in the initiate state;  
8           a test state entered into from the flush state; and  
9           a done state entered into upon completing the test of each of a plurality of memory  
10          components in the memory built-in self-test.

1           11.      The built-in self-test controller of claim 9, wherein the memory built-in self-  
2 test engine comprises:

3           a plurality of alternative memory built-in self-test state machines; and  
4           a nested memory built-in self-test engine operating a predetermined one of the  
5           memory built-in self-test state machines.

1           12.      The built-in self-test controller of claim 11, wherein each of the memory built-  
2 in self-test engines comprises:

3 a reset state entered upon receipt of an external reset signal;  
4 an initiate state entered from the reset state upon receipt of at least one of a memory  
5 built-in self-test run signal and a memory built-in self-test select signal;  
6 a flush state entered from the initiate state upon the initialization of components and  
7 signals in the memory built-in self-test domain in the initiate state;  
8 a test state entered into from the flush state; and  
9 a done state entered into upon completing the test of each of a plurality of memory  
10 components in the memory built-in self-test.

1 13. A built-in self-test controller, comprising:  
2 means for executing a built-in self-test and generating an indication of whether the  
3 executed built-in self-test is completed; and  
4 means for storing the results of the executed built-in self-test, including the indication.

5 14. The built-in self-test controller of claim 13, wherein the executing means is a  
6 logic built-in self-test engine and the storing means is a logic built-in self-test register.

7 15. The built-in self-test controller of claim 13, wherein the storing means  
8 comprises the content of a multiple input signature register.

9 16. The built-in self-test controller of claim 13, wherein the executing means is a  
10 memory built-in self-test engine and the storing means is a memory built-in self-test signature  
11 register.

1 17. An integrated circuit device, comprising:  
2 a plurality of memory components;  
3 a logic core;  
4 a testing interface; and  
5 a built-in self-test controller, including:  
6 a built-in self-test engine capable of executing a built-in self-test on one of the  
7 memory components and the logic core and storing the results thereof,  
8 wherein the results include an indication of whether an executed built-  
9 in self-test is completed; and  
10 a register capable of storing the results of an executed built-in self-test,  
11 including the indication.

18. The integrated circuit device of claim 17, wherein the built-in self-test engine is a logic built-in self-test engine and the register is a multiple input signature register.

19. The integrated circuit device of claim 17, wherein the built-in self-test engine is a memory built-in self-test engine and the register is a memory built-in self-test signature register.

20. The integrated circuit device of claim 17, wherein the memory components include a static random access memory device.

21. The integrated circuit device of claim 17, wherein testing interface comprises a Joint Test Action Group tap controller.

22. A method for performing a built-in self-test, the method comprising:  
performing a built-in self-test, including generating a indication of whether the built-in self-test is completed; and  
storing the indication.

23. The method of claim 22, wherein performing the built-in self-test includes performing a logic built-in self-test and storing the indication includes setting a bit in a multiple input signature register.

24. The method of claim 23, wherein performing the logic built-in self-test includes:

resetting a logic built-in self-test engine;  
initiating a plurality of components and signals in a built-in self-test controller upon receipt of a logic built-in self-test run signal;  
scanning a scan chain upon the initialization of the components and the signals;  
stepping to a new scan chain; and  
repeating the previous scanning and stepping until the content of a pattern generator in a logic built-in self-test engine of the built-in self-test controller equals a predetermined vector count.

25. The method of claim 23, further comprising at least one of:  
setting a bit in the multiple input signature register indicating an error condition arose;  
and

4 setting a bit in the multiple input signature register indicating whether the stored  
5 results are from a previous logic built-in self-test run.

1 26. The method of claim 22, wherein performing the built-in self-test includes  
2 performing a memory built-in self-test and storing the indication includes setting a bit in a  
3 memory built-in self-test signature register.

1 27. The method of claim 26, wherein performing the memory built-in self-test  
2 includes:

3 resetting a memory built-in self-test engine;  
4 initiating a plurality of components and signals in a built-in self-test controller upon  
5 receipt of at least one of a memory built-in self-test run signal and a memory  
6 built-in self-test select signal;  
7 flushing the contents of a plurality of memory components to a known state after  
8 initialization of the components and the signals; and  
9 testing the flushed memory components.

1 28. The method of claim 26, wherein performing the memory built-in self-test  
2 further includes at least one of:

3 storing the results of the memory built-in self-test in the memory built-in self-test  
4 signature register; and  
5 storing the results of at least one paranoid check in the memory built-in self-test  
6 signature register.

1 29. A method for testing an integrated circuit device, the method comprising:  
2 interfacing the integrated circuit device with a tester;  
3 performing a built-in self-test, including generating a indication of whether the built-  
4 in self-test is completed;  
5 storing the indication; and  
6 reading the indication.

1 30. The method of claim 29, wherein performing the built-in self-test includes  
2 performing a logic built-in self-test and storing the indication includes setting a bit in a  
3 multiple input signature register.

1           31.     The method of claim 29, wherein performing the built-in self-test includes  
2 performing a memory built-in self-test and storing the indication includes setting a bit in a  
3 memory built-in self-test signature register.

1           32.     The method of claim 29, wherein interfacing the integrated circuit device with  
2 the tester includes employing Joint Test Action Group protocols.

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